Notice of Allowability	Application No.	Applicant(s)	
	10/692,103	VINING, SUZANNE MARY	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdts filed 08/14/06*.

2. ☒ The allowed claim(s) is/are *1-23*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *10/15/06* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and or additions be acceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no latter than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Dennis Moore on 10/15/06.

2. The application has been amended as follows:

As per claims 8, 14, and 18:

Change phrase or word "NRZI" to ---Non-Return-to-Zero Inverted (NRZI)---(see line 2 and 3 of claims 1, 8, 14 and 18).

As per claim 8:

Change the paragraph "a phase generator that produces N phases of a clock signal that has an associated frequency of approximately the same frequency of the received serial data stream, wherein the N phases are successively offset by (1/N) of a time period; and to ---a phase generator that produces N phases of a clock signal that has an associated frequency that deviates from the frequency of the received serial data stream, by no more than a predetermined range, wherein the N phases are successively offset by (1/N) of a time period;---.

Examiner's statement for reason for allowance

3. Claims **1-23** have been allowed.

The following is an examiner's statement for allowance:

As per claim 1:

The prior art of record Maddux substantially discloses (Fig. 1. element 150) a data recovery device (col. 1, lines 7-9) comprising a number of sample components (block 230 of Fig. 2) that obtain (or generate) samples (d1 ...dN) of a received serial data stream (115) at a number of phases (231), wherein the number of phases are successively offset (column 3, lines 37-41) throughout a bit time period and the samples are obtained throughout the time period at the number of phases (N different phases; a number of transition detectors (Maddux uses the term "edge detector", block 250 of Fig. 2) corresponding to the number of obtained samples that analyze consecutive data samples in order to identify transitions (column 3, lines 45-*, and a first circuit (including logic blocks 240 and/or 280 as compared to the OR gate 508 of the inventive Fig. 5A) that generates a serial decoded data stream (recovered data) that comprises values for time periods) according to occurrence or non occurrence of one or more transitions within the respective time periods. Millar (U.S. PN: 6,337,590) teaches a toggling operation and ensures that a shift register responds quickly to the need to find the phase detection region and lock condition whereby during this time, a jitter filter is inhibited (blocked) from operating and once the lock condition has been established and the jitter filter has been enabled by the output of flip-flop being logic 0, a sync flip-flop changes operating modes to operate in the interval mode whereby a CLKS pulse is generated every 127 CLKR pulses. Thus the flip-flop activates the clock jitter filter once the delay locked loop has detected an initial phase match condition (see col. 8, lines 57-67 and col. 9, lines 1-9). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious clock recovery device comprising a number

of sample components that obtain samples of a received NRZI encoded serial data stream at a number of phases, respectively, wherein the number of phases are successively offset throughout a bit time period and the samples are obtained throughout the time period at the number of phases; a number of transition detectors corresponding to the number of obtained samples that analyze consecutive data samples in order to identify transitions; a continuously operating blocking component that selectively blocks clock phases phase which were selected for a prior transition that would erroneously contribute the final recovered clock if not blocked, while allowing clock phases which were selected for a prior transition and that do not erroneously contribute to the final recovered clock, and a select clock component that selects a clock phase according to a the data toggle phase and generates a selected clock. Consequently, claim 1 is allowed over the prior art.

Claims **2-7,** which is/are directly or indirectly dependent/s of claim 1 are also allowable over the prior art of record.

As per claim 8:

The prior art of record Maddux substantially discloses (Fig. 1. element 150) a data recovery device (col. 1, lines 7-9) comprising a number of sample components (block 230 of Fig. 2) that obtain (or generate) samples (d1 ...dN) of a received serial data stream (115) at a number of phases (231), wherein the number of phases are successively offset (column 3, lines 37-41) throughout a bit time period and the samples are obtained throughout the time period at the number of phases (N different phases; a number of transition detectors (Maddux uses the term "edge detector", block 250 of Fig. 2) corresponding to the number of obtained samples that analyze consecutive data samples in order to identify transitions (column 3, lines 45-*, and a first

circuit (including logic blocks 240 and/or 280 as compared to the OR gate 508 of the inventive Fig. 5A) that generates a serial decoded data stream (recovered data) that comprises values for time periods) according to occurrence or non occurrence of one or more transitions within the respective time periods. Millar (U.S. PN: 6,337,590) teaches a toggling operation and ensures that a shift register responds quickly to the need to find the phase detection region and lock condition whereby during this time, a jitter filter is inhibited (blocked) from operating and once the lock condition has been established and the jitter filter has been enabled by the output of flip-flop being logic 0, a sync flip-flop changes operating modes to operate in the interval mode whereby a CLKS pulse is generated every 127 CLKR pulses. Thus the flip-flop activates the clock jitter filter once the delay locked loop has detected an initial phase match condition (see col. 8, lines 57-67 and col. 9, lines 1-9). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious clock recovery device comprising a clock and data recovery system comprising: a receiver that receives an NRZI encoded serial data stream having an associated frequency; a phase generator that produces N phases of a clock signal that has have an associated frequency of **approximately** the same as the frequency of the received serial data stream, wherein the N phases are successively offset by (l/N) of a time period; and a clock recovery component that identifies transitions in the received serial data stream, selects a clock phase from a first identified transition of a bit time, blocks one other stale selected clock phase, and selects an appropriate e clock accordingly. Consequently, claim 8 is allowed over the prior art.

Claims **9-13,** which is/are directly or indirectly dependent/s of claim 8 are also allowable over the prior art of record.

As per claim 14:

The prior art of record Maddux substantially discloses (Fig. 1. element 150) a data recovery device (col. 1, lines 7-9) comprising a number of sample components (block 230 of Fig. 2) that obtain (or generate) samples (d1 ...dN) of a received serial data stream (115) at a number of phases (231), wherein the number of phases are successively offset (column 3, lines 37-41) throughout a bit time period and the samples are obtained throughout the time period at the number of phases (N different phases; a number of transition detectors (Maddux uses the term "edge detector", block 250 of Fig. 2) corresponding to the number of obtained samples that analyze consecutive data samples in order to identify transitions (column 3, lines 45-*, and a first circuit (including logic blocks 240 and/or 280 as compared to the OR gate 508 of the inventive Fig. 5A) that generates a serial decoded data stream (recovered data) that comprises values for time periods) according to occurrence or non occurrence of one or more transitions within the respective time periods. Millar (U.S. PN: 6,337,590) teaches a toggling operation and ensures that a shift register responds quickly to the need to find the phase detection region and lock condition whereby during this time, a jitter filter is inhibited (blocked) from operating and once the lock condition has been established and the jitter filter has been enabled by the output of flip-flop being logic 0, a sync flip-flop changes operating modes to operate in the interval mode whereby a CLKS pulse is generated every 127 CLKR pulses. Thus the flip-flop activates the clock jitter filter once the delay locked loop has detected an initial phase match condition (see col. 8, lines 57-67 and col. 9, lines 1-9). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a clock recovery system comprising: a number of phase components that respectively obtain data samples of an NRZI encoded serial

data stream, identify transitions, set a toggle bit per transition, select a clock phase based on a prior phase toggle setting, use the preceding toggle to block the current clock phase, and generate a clock; and a clock selector that generates a recovered clock from the clocks generated by the number of phase components. Consequently, claim 14 is allowed over the prior art.

Claims **15-17** which is/are directly or indirectly dependent/s of claim 14 are also allowable over the prior art of record.

As per claim 18:

The prior art of record Maddux substantially discloses (Fig. 1. element 150) a data recovery device (col. 1, lines 7-9) comprising a number of sample components (block 230 of Fig. 2) that obtain (or generate) samples (d1 ...dN) of a received serial data stream (115) at a number of phases (231), wherein the number of phases are successively offset (column 3, lines 37-41) throughout a bit time period and the samples are obtained throughout the time period at the number of phases (N different phases; a number of transition detectors (Maddux uses the term "edge detector", block 250 of Fig. 2) corresponding to the number of obtained samples that analyze consecutive data samples in order to identify transitions (column 3, lines 45-*, and a first circuit (including logic blocks 240 and/or 280 as compared to the OR gate 508 of the inventive Fig. 5A) that generates a serial decoded data stream (recovered data) that comprises values for time periods) according to occurrence or non occurrence of one or more transitions within the respective time periods. Millar (U.S. PN: 6,337,590) teaches a toggling operation and ensures that a shift register responds quickly to the need to find the phase detection region and lock condition whereby during this time, a jitter filter is inhibited (blocked) from operating and once the lock condition has been established and the jitter filter has been enabled by the output of flip-

flop being logic 0, a sync flip-flop changes operating modes to operate in the interval mode whereby a CLKS pulse is generated every 127 CLKR pulses. Thus the flip-flop activates the clock jitter filter once the delay locked loop has detected an initial phase match condition (see col. 8, lines 57-67 and col. 9, lines 1-9). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a method of recovering data over a single time period comprising: obtaining a number of data samples of a received NRZI encoded serial data stream according to a number of phase clocks; analyzing consecutive data samples to identify transitions; setting a toggle phase according to a first identified transition of a current bit time; blocking one subsequent phase from being selected as a clock; and selecting a clock phase according to the toggle phase. Consequently, claim 18 is allowed over the prior art.

Claims **19-23**, which is/are directly or indirectly dependent/s of claim 18 are also allowable over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned (571) 273-8300.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

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Art unit: 2133

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